RN.2 Technologies

Datasheet

CXD21P02

Rev. 1.2

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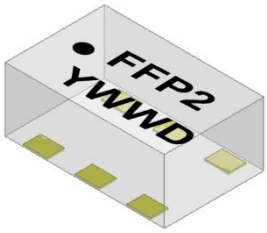
2-Way Divider
with High-Power Capacity and Stable Performance based on RN2 LTCC Multilayer Technology
Model Name: CXD21P02

1. KEY FEATURES

- Excellent high-power capacity up to average 2 watts
- Excellent stable performance at different temperatures
- Low insertion loss based on a LTCC base (Er = 5.95), high conductivity metal conductor (Ag), and gold (Au) plating
- Surface mount type
- RoHS compliance (Pb-Free)



2. APPLICATIONS

- Applications using GSM, UMTS, and LTE
- RF amplifiers
- Communications equipment

3. GENERAL DESCRIPTIONS

The CXD21P02 is a 2-way divider with high-power capacity and stable performance in different temperatures. The LTCC, high conductivity metal conductor (Ag), and gold (Au) plating enable the CXD21P02 to minimize insertion loss and improve durability for thermal stabilization and electricity.

The CXD21P02 is suited for applications using GSM, UMTS, LTE, communications equipment, requiring low insertion loss and high power.

The CXD21P02 supports up to average 2 watts. It is a SMD type product enabling Pb-Free solder and meets RoHS-6.

4. ELECTRICAL SPECIFICATIONS

Frequency (MHz)	Amplitude Balance Max.(dB)	Isolation Min.(dB)	Insertion Loss Max.(dB)
1700-2200	± 0.30	18	0.6
Return Loss Min.(dB) Input / Output	**Phase Balance (Degrees)**	**Power Capacity Avg.(Watt)**	**Operating Temperature(℃)**
13 / 20	0 ± 1.0	2	-55 ~ + 125

NOTE: These electrical specifications are measured by using a RN2 test board.
Specifications subject to change without notice.

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5. PORT CONFIGURATIONS

Figure 1 shows the locations of the CXD21P02 ports. The orientation marker is included to represent port 1.

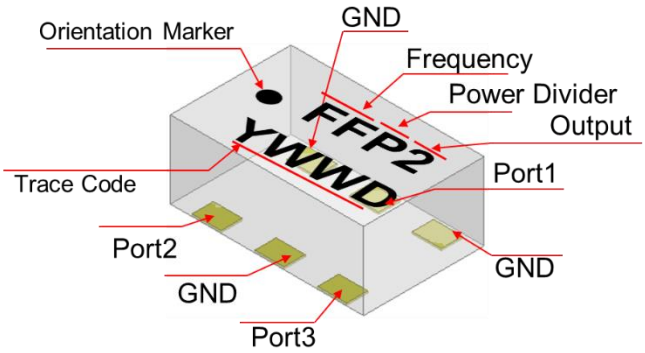


Figure 1. CXD21P02 (Top View)

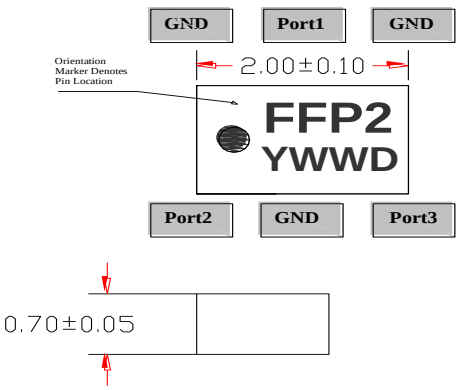
CXD21P02 port configuration is defined as table1.

Table 1. CXD21P02 Port Configurations

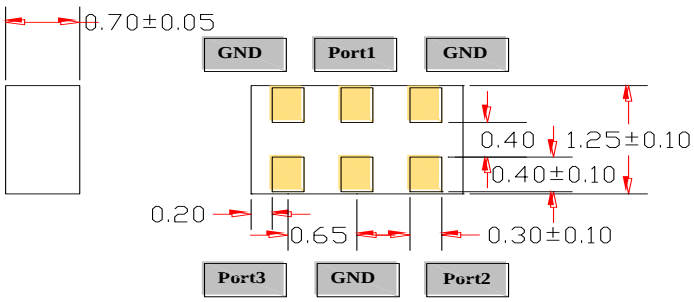
Configuration	Port 1	Port 2	Port 3
Case 1.	Input	Output1	Output2

6. OUT DIMENSION

Top View



Bottom View



- Unit: mm
- Weight: 0.01 grams
- Camber specifications: Less than 0.08 mm

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7. POWER DERATING CURVE

Figure 2 shows the maximum allowable average power (Maximum input power, CW) of the CXD21P02 depending on base PCB temperature changes. The maximum allowable average power of the CXD21P02 is limited by the following power derating curve.

The CXD21P02 factors that determine the power derating curve are as follows:

- Internal circuit
- Thickness
- Thermal conductivity of materials
- Insertion loss
- Operating temperature
- Mounting interface temperature between the CXD21P02 and the base PCB

The maximum operating temperature of the CXD21P02 is 125 ºC. Therefore, when the base PCB temperature is over 125 ºC, the CXD21P02 operates stably by decreasing its durable average input power. When the base PCB temperature reaches 200 ºC, the maximum allowable average power decreases to 0 watt.

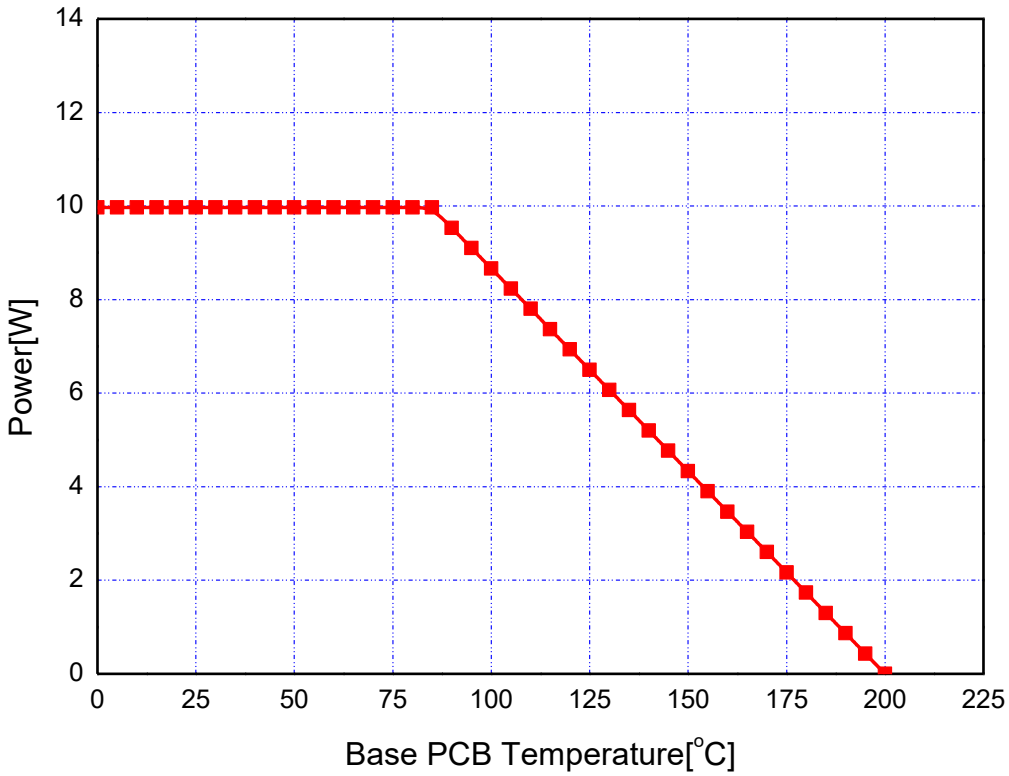

Figure 2. Power Derating Curve

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8. RF PERFORMANCE CURVES: Return Loss (-55 ºC, 25 ºC, and 125 ºC)

Figure 3 shows the test plots of the return loss for the CXD21P02. There are few variations for the specified frequencies and temperatures.

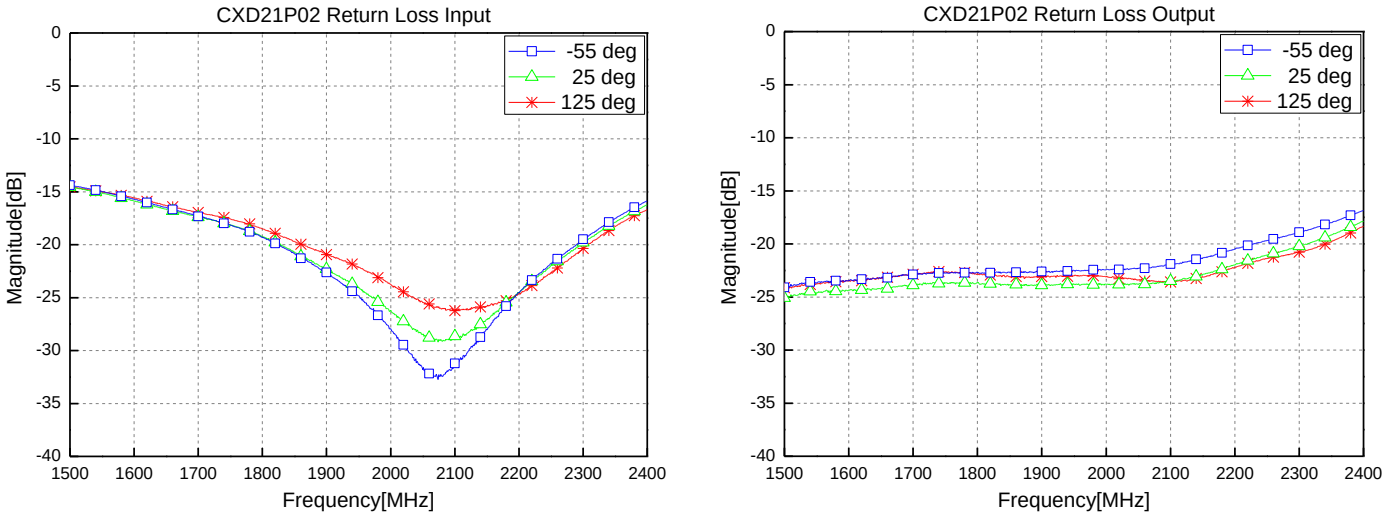

Figure 3. Test Plots of Return Loss (-55 ºC, 25 ºC, and 125 ºC)

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9. RF PERFORMANCE CURVES: Amplitude Balance, Insertion Loss, Isolation, and Phase Balance (-55 ºC, 25 ºC, and 125 ºC)

Figure 4 shows the test plots of the insertion loss, isolation, amplitude balance, and phase balance for the CXD21P02. There are few variations for the specified frequencies and temperatures. These test plots result from the Case 1 configuration in *'Table 1. CXD21P02 Port Configurations'*. See *'PORT CONFIGURATIONS'* for more details.

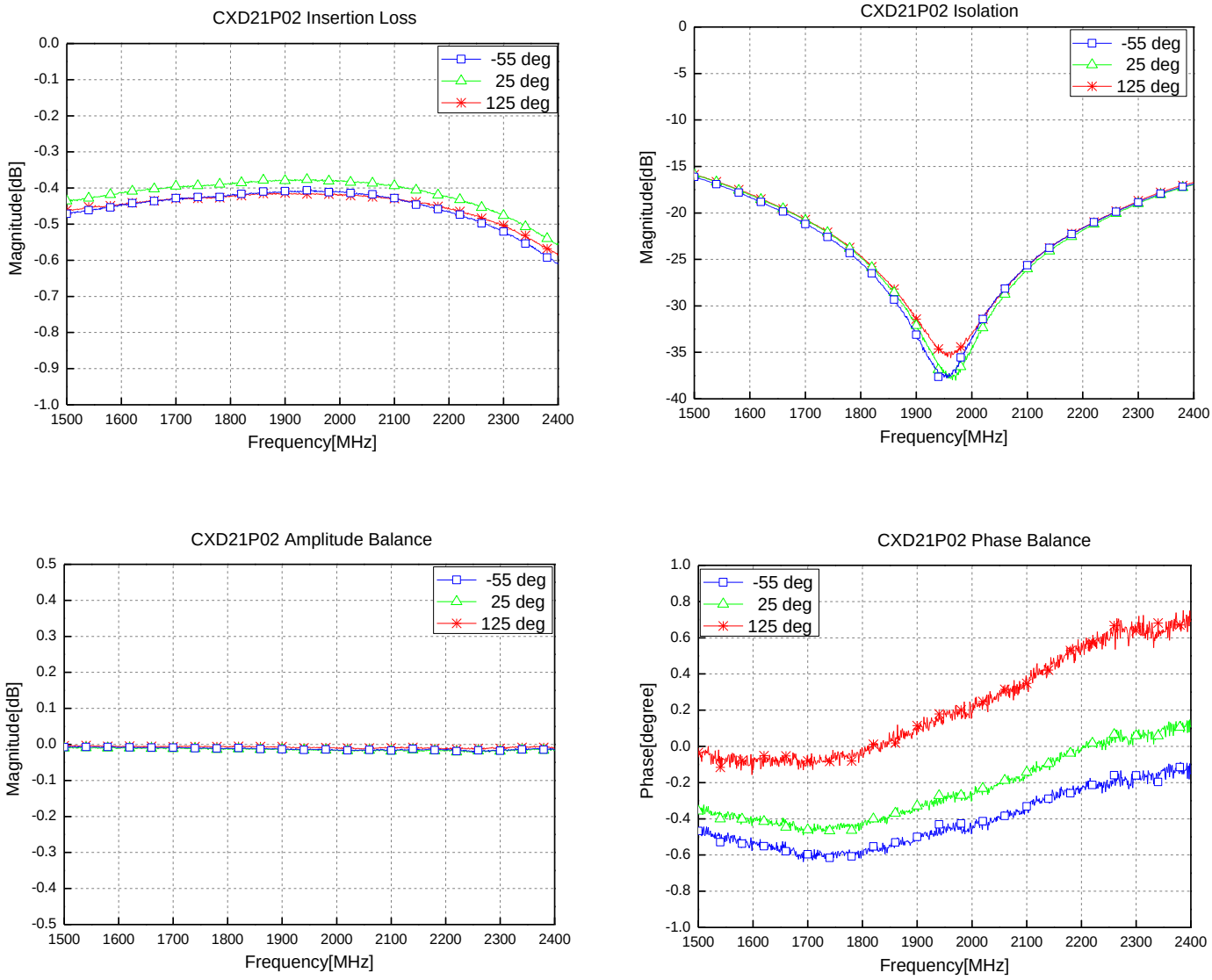

Figure 4. Test Plots of Coupling and Transmission Loss, Insertion Loss, Isolation, and Phase Balance (-55 ºC, 25 ºC, and 125 ºC)

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10. RF TEST METHODS

This section describes how to test the CXD21P02 RF performance. To ensure s-parameters reliability, we follow our internal test procedures by using the RN2 bare test board, RN2 test board, Vector network analyzer, and test fixture. In addition, we use the Automatic Port Extensions (APE) function of the Vector network analyzer to obtain accurate s-parameters.

Check the following sections for more details:

- RF TEST PROCEDURES
- RN2 TEST BOARD LAYOUT
- AUTOMATIC PORT EXTENSIONS (APE) FUNCTION

10.1 RF TEST PROCEDURES

To test the CXD21P02 RF performance, we perform the following steps:

1. Preparing the Test Equipment
2. Performing the Automatic Port Extensions (APE) Function of the Vector Network Analyzer
3. Measuring the S-parameters (Isolation, and Return Loss)
4. Obtaining the Characteristic Parameters (Amplitude Balance, Isolation, Insertion Loss, Return Loss, and Phase Balance)

STEP 1: Preparing the Test Equipment
The following test equipment is prepared to test the CXD21P02 RF performance.

- RN2 bare test board
- RN2 test board
- Vector network analyzer
- Test fixture

NOTE: See *'RN2 TEST BOARD LAYOUT'* for the RN2 test board details.

STEP 2: Performing the Automatic Port Extensions (APE) Function of the Vector Network Analyzer
The APE function is used with the RN2 bare test board to correctly check the CXD21P02 RF performance. This reduces or eliminates both electrical delay and insertion loss of the test fixture.

The detailed steps are as follows:

1. Place the RN2 bare test board on the text fixture.
2. Click the **Cal** button of the Vector network analyzer to calibrate it.
3. Connect the three ports of the test fixture into the three ports of the Vector network analyzer.
4. Click the **Port Extensions** button of the Vector network analyzer to measure the data of the RN2 bare test board.

NOTE: See *'AUTOMATIC PORT EXTENSIONS FUNCTION'* for more details.

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STEP 3: Measuring the S-parameters (Coupling, Transmission Loss, Isolation, and Return Loss)

After performing the APE function, the CXD21P02 s-parameters are measured through the following steps:

1. Place the RN2 test board on the text fixture.
2. Apply pressure to the text fixture using a pneumatic piston.
3. Connect the four ports of the test fixture into the fours ports of the Vector network analyzer.
4. Set port1 as Case 1 configuration in *'Table 1. CXD21P02 Port Configurations'*.
5. Calibrate the Vector network analyzer.
6. Measure the isolation value from port 2 to port 3 (S32).
7. Measure the return loss value from port 1 to port 1, port 2 to port 2, and port 3 to port 3 respectively (S11, S22, and S33).

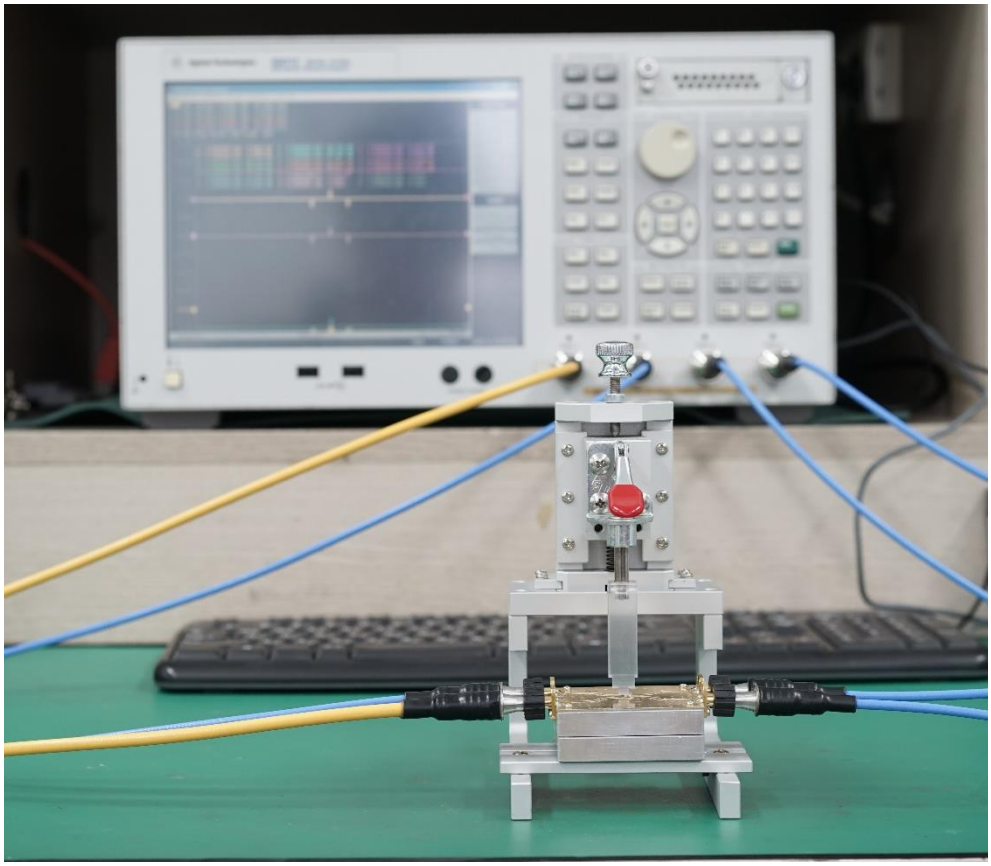

Figure 5. Test Setting to Measure the CXD21P02 S-parameters

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STEP 4: Obtaining the Characteristic Parameters (Amplitude Balance, Isolation, Insertion Loss, Return Loss, and Phase Balance)

The s-parameters are calculated by using the formula in ***Table 2*** to obtain the characteristic parameters, such as amplitude balance, isolation, insertion loss, return loss, and phase balance.

Table 2. Mathematical Formula for the CXD21P02 Parameters

Parameter	S-Parameter	Power Method
Insertion Loss	-	$10 \cdot \log\left(\frac{P_{in}}{P_{out1} + P_{out2}}\right)$
Isolation	S32	$10 \cdot \log\left(\frac{P_{iso}}{P_{in}}\right)$
Return Loss	S11 S22 S33	$10 \cdot \log\left(\frac{P_{in}}{P_{back}}\right)$
Amplitude Balance	-	$10 \cdot \log\left(P_{out1} \Big/ \frac{P_{out1} + P_{out2}}{2}\right)$
Phase Balance	S21 S31	$\text{Phase}_{(S21)} - \text{Phase}_{(S31)}$

NOTE

- P_{in} : Power of Input Port
- P_{out} : Power of Output Port
- P_{back} : Return Power of Input Port

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10.2 RN2 TEST BOARD LAYOUT

Figure 6 shows the RN2 test board layout used for testing the CXD21P02 RF performance. The RN2 test board is based on the Taconic RF35 board with the dielectric constant of 3.5, board thickness of 0.8 mm, and copper of 1 Oz.

We recommend that you use the same material and design layout, as shown in ***Figure 6***, to meet the specifications in this datasheet. However, if you use different materials, you must follow the basic guidelines. See *'RECOMMENDED PCB LAYOUT AND SOLDER MASK PATTERN'* for more details.

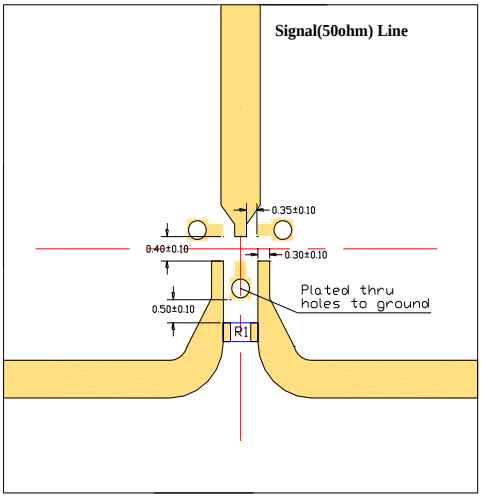

Figure 6. RN2 Test Board Layout

10.3 AUTOMATIC PORT EXTENSIONS (APE) FUNCTION

To accurately measure the CXD21P02 s-parameters, we use the Automatic Port Extensions (APE) function of the Vector network analyzer. The APE function is used for reducing or eliminating both electrical delay and insertion loss of test fixtures. It provides a convenient, automated way to calculate the insertion loss and electrical delay terms by a simple measurement of an open or short circuit, which is easy to do in test fixtures.

We consider the transmission lines of the RN2 bare test board as extensions of the coaxial test cables that are between the Vector network analyzer and the CXD21P02. With the APE function, we extend the coaxial test ports so that our calibration plane is right at the terminals of the CXD21P02, and not at the connectors of the RN2 bare test board.

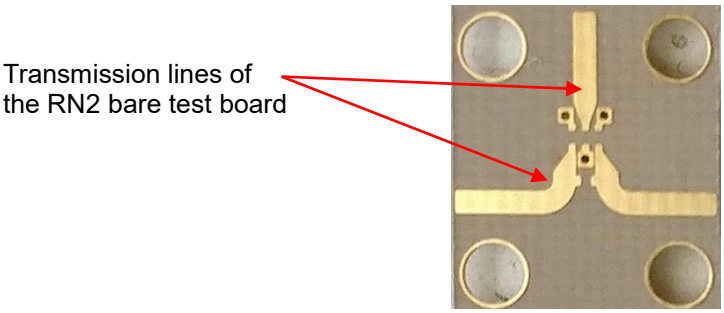

Figure 7. Performing the APE Function Test

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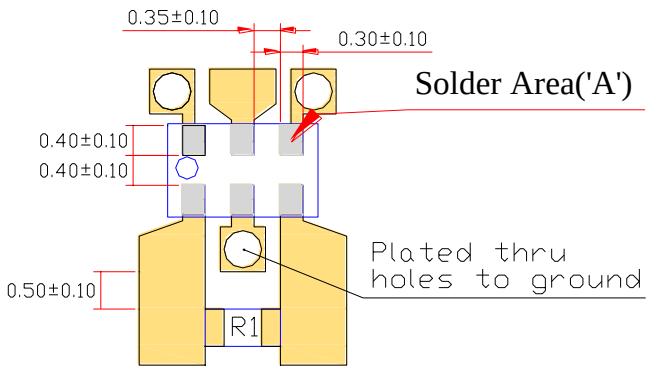
11. RECOMMENDED PCB LAYOUT AND SOLDER MASK PATTERN

Figure 8 shows the recommended PCB layout and solder mask pattern to meet the specifications in this datasheet. When you use different materials other than the RN2 test board, you must follow the basic guidelines at minimum.

Basic Guidelines

- Place GND more than 30% of the CXD21P02 GND dimension regardless of a via size.
- Appropriately increase via sizes and numbers to allow low impedance ground connection and good thermal conductivity.
- Align the CXD21P02 ground plane with the solder to have good connection to ground.
- Fill the via holes under the CXD21P02 with the solder for thermal emission.

NOTE: Contact the RN2 Technologies sales team for more detailed PCB layout and solder mask pattern information.



NOTE

- Test Solder Cream: SAC-305 (Alpha Metal)
- Pb-Free Solder Alloy: Sn/Ag/Cu Ratio of 96.5/3.0/0.5
- Solder Area ('A') Dimension : 0.33 mm by 0.33 mm
- R1 : 100Ω

Figure 8. Recommended PCB Layout and Solder Mask Pattern

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12. SOLDERING PROCESS

The CXD21P02 soldering steps are as follows:

1. Cleaning the PCB
2. Applying solder paste to the PCB
3. Placing the CXD21P02 on the PCB
4. Reflowing the CXD21P02 to the PCB
5. Cleaning and inspecting the soldered PCB with the CXD21P02

STEP 1: Cleaning the PCB
Carefully clean the PCB surface where the CXD21P02 is soldered.
Particles must not be placed on the PCB surface where the CXD21P02 is soldered.

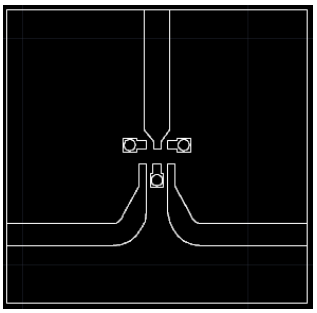

Figure 9. Cleaning the PCB Surface Where the CXD21P02 is Soldered

STEP 2: Applying the Solder Paste to the PCB
Apply the solder paste to the 6points on the PCB surface.
It enables good thermal conductivity because the CXD21P02 is firmly attached to the PCB surface without air.

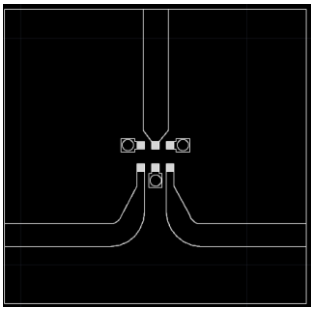

Figure 10. Applying the Solder Paste to the 6Points on the PCB Surface

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STEP 3: Placing the CXD21P02 on the PCB
Correctly place the CXD21P02 on the 6points of the PCB surface.
Applying the solder paste to the 6points helps you firmly attach the CXD21P02 to the PCB surface.

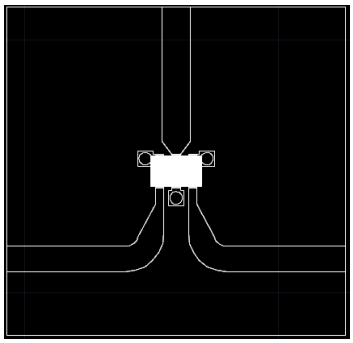

Figure 11. Placing the CXD21P02 on the 6Points of the PCB Surface

STEP 4: Reflowing the CXD21P02 to the PCB
We recommend both manual soldering and PCB surface pre-heating methods when reflowing the CXD21P02 to the PCB surface. Be careful NOT to touch the iron tip to the CXD21P02 when you use the manual soldering method.
See *'REFLOW PROFILE'* for more details.

13. REFLOW PROFILE

Figure 12 shows the thermal reflow profile of the SAC-305 (Alpha metal), which is a test solder cream we used.

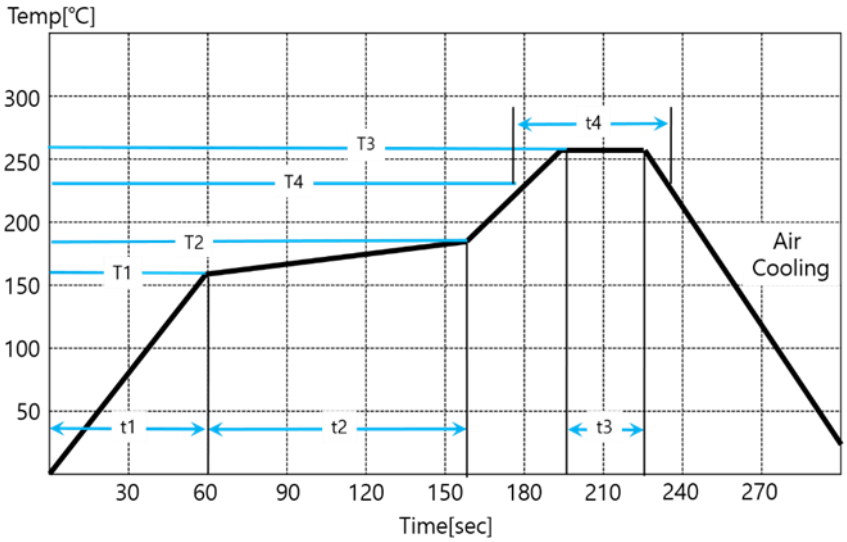

Figure 12. Thermal Reflow Profile

	Ramp Up	Pre-Heating	Peak	Soaking
Temperature(℃)	T1:160±5	T2:180±5	T3:260±5	T4:230±5
Time(sec)	t1:60±5	t2:100±15	t3:30±5	t4:60±10

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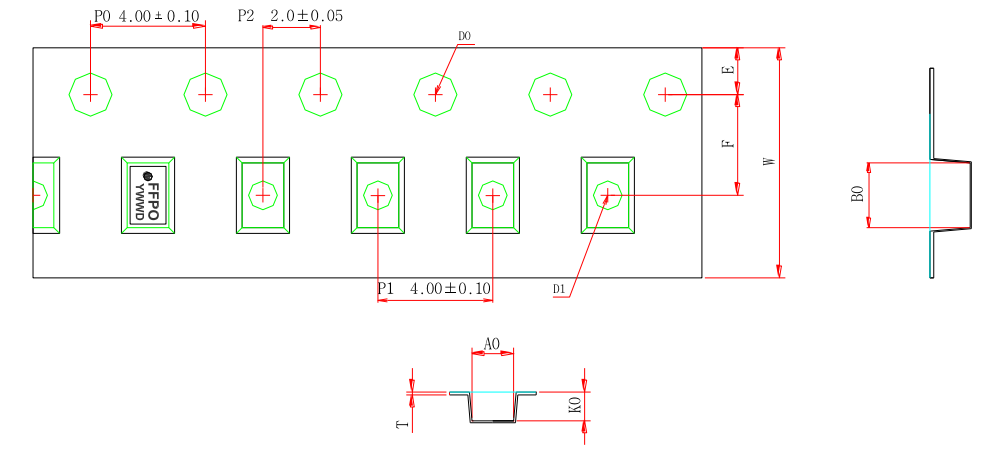

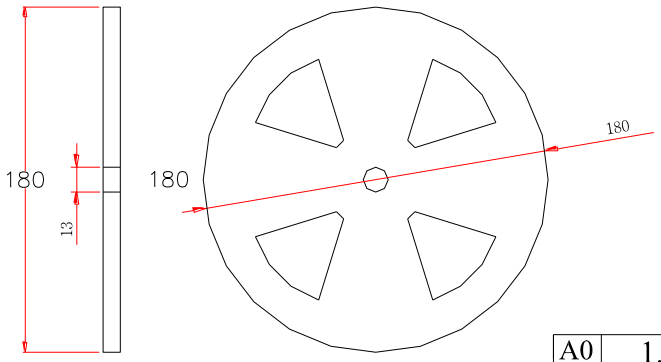

[Unit: mm]

A0	1.50±0.05	E	1.75±0.10
B0	2.25±0.05	F	3.50±0.05
D0	1.55±0.05	T	0.25±0.03
K0	1.00±0.10	W	8.00±0.30

Starndard Packaging Quantity : 3,000 PCS / Reel

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15. HANDLING GUIDE

PLEASE READ THIS NOTICE BEFORE USING OUR LTCC DIVIDERS.

I. Be careful when transporting

- Ensure proper transportation as excessive stress or shock may damage LTCC dividers due to the nature of ceramics structure.
- LTCC dividers cracked or damaged on terminals may have their property changed.

II. Be careful during storage

- Store LTCC couplers less than temperature +30°C.
- Keep the humidity at 45% to 75% around LTCC dividers.
- Prevent corrosive gas (Cl_2, NH_3, SO_X, NO_X, etc.) from contacting LTCC dividers.
- It is recommended to use LTCC dividers within 6 months of receipt. If the period exceeds 6 months, solderability may need to be verified.

III. Be careful when soldering

- Solder all the ground terminals, IN and OUT pad of LTCC dividers on the ground plane of the PCB.
- LTCC dividers may be cracked or broken by uneven forces from a claw or suction device.
- Mechanical stress by any other devices may damage LTCC dividers when positioning them on PCB.
- Do not use dropped LTCC dividers.
- Ensure that any soldering is carried out by the condition of specification sheet.
- Do not re-use LTCC dividers which are de-soldered from PCB.

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